The University of Tokushima (2011)⟩ Graduate School of Advanced Technology and Science⟩ Electrical and Electronic Engineering (Doctor) [⇒Japanese]

2 units (selection)

Minoru Fukumi · Professor / Information Science, Information Science and Intelligent Systems, Systems Innovation Engineering

- Takashi Shimamoto · Professor / Intelligent Networks and Computer Science, Electrical and Electronic Engineering, Systems Innovation Engineering
- **Target**> The aim of this lecture is to master the modern design technologies of very large scale integrated circuits.
- **Outline**> Very large scale integrated circuit (V-LSI) design and production method. Using CAD technology, VLSI logic design, testing and fabrication are explained. Design of high-speed algorithm and parallel distributed processing system. Neural network and genetic algorithm for integrated circuit design.

Style> Lecture and excercise

- **Requirement**> It is necessary to get the unit of the mos integrated circuits in master cource.
- **Notice**) In order to get the unit of this lecture, the grduate cource students should have learned the-state-of-the-art of the modern hardware technology, especially C-MOS integrated circuits.
- **Goal**> This lecture is desighted to provide engineers and scientists with an introduction to the fieled of VLSI neurocomputing.

$\textbf{Schedule}\rangle$

- 1. Embedded software architecture
- 2. Real-time schedure method
- **3.** System description language
- 4. Application specific integrated circuits
- 5. Power consumption and speed of very large scale integrated circuits
- 6. Shared memory and communication mrthod

Integrated Information System Design

- 7. Cash memory and main memory
- 8. System modeling and documentation
- 9. Partitioning and performance
- 10. deta flow graph and finite state machine
- **11.** Behavior description language and Spec C
- **12.** Control deta-flow graph and function synthesis
- 13. Neural computing board diagram using EEPROM-style programmable synapses
- **14.** Layout patern example
- 15. Gate-sizing wiring and timing driven
- 16. Boundary scan and delay estimation

Evaluation Criteria Unit evaluation contains test and design of VLSI

- **Textbook**> Hardware Annealing in Analog VLSI Neurocomputing, Kluer Academic Publishers
- Reference Electronics Circuits, written by Norio Akamatsu
- Webpage http://titan.is.tokushima-u.ac.jp/~fukumi
- Contents http://cms.db.tokushima-u.ac.jp/cgi-bin/toURL?EID=216700
- Student) Able to be taken by student of other department and faculty

Contact>

- ⇒ Fukumi (D210, +81-88-656-7510, fukumi@is.tokushima-u.ac.jp) MAIL (Office Hour: 原則として, 水曜日 15 時~18 時, ただし年度により異なる 場合があるので講義の際に指定する.)
- Note> Lecturer will show the schedule of this lecture and design technologies.